TFA9810

Stereo full-bridge audio amplifier 2 x 12 W

Rev. 02 — 30 August 2007 Preliminary data sheet

1. General description

The TFA9810 is a two-channel power comparator for high-efficiency class D audio amplifier systems. It contains two full-bridge Bridge-Tied Load (BTL) power stages, drive logic, protection control logic and full differential input comparators. By using this power comparator a compact closed-loop self-oscillating digital amplifier system or open-loop system can be built. The TFA9810 does not require a heat sink and operates using an asymmetrical supply voltage.

2. Features

- Stereo full-bridge power comparator for class D audio amplifier applications
- No external heat sink required
- Operating voltage range: asymmetrical from 8 V to 20 V
- Thermally protected
- Zero dead-time switching
- Current-limiting (no audible interruptions)

3. Applications

- Self-oscillating or open-loop class D audio amplifier applications
- Flat-panel television sets
- Flat-panel monitors
- Multimedia systems
- Wireless speakers
- High-end CRT television sets

4. Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C; V_P = 12 V; f_{osc} = 550 kHz; Figure 33 unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_P	supply voltage	$V_P = V_{DDPx} - V_{SSPx}$	8	12	20	V
I_{off}	off-state current	Off mode	-	110	200	µA
I_q	quiescent current	With load, filter and snubbers connected	-	35	45	mA
η_{po}	output power efficiency	Output power 2 x 9 W into 8 Ω; $P_o = P_{o(nom)}$	87	89	-	%

Table 1. Quick reference data *...continued*

T_{amb} = 25 °C; V_P = 12 V; f_{osc} = 550 kHz; Figure 33 unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$P_{o(RMS)}$	continuous RMS output power per channel	R_L = 8 Ω; 12 V; THD = 10 %; Two channel driven; no heat sink required.	-	9.5	-	W
P_o	output power	V_P =12 V; R_L = 8 Ω	-	-	-	-
		THD = 10 %	8.5	9.5	-	W
		THD = 1 %	6.5	7.5	-	W
		V_P =14 V; R_L = 8 Ω; THD = 10 %; thermally limited	-	15	-	W
		V_P =16 V; R_L = 8 Ω; THD = 10 %; thermally limited	-	15	-	W
		V_P = 12 V; R_L = 6 Ω; THD = 10 %; thermally limited	-	12	-	W
		V_P = 12 V; R_L = 4 Ω; THD = 10 %; thermally limited	-	12	-	W

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9810T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

6. Block diagram

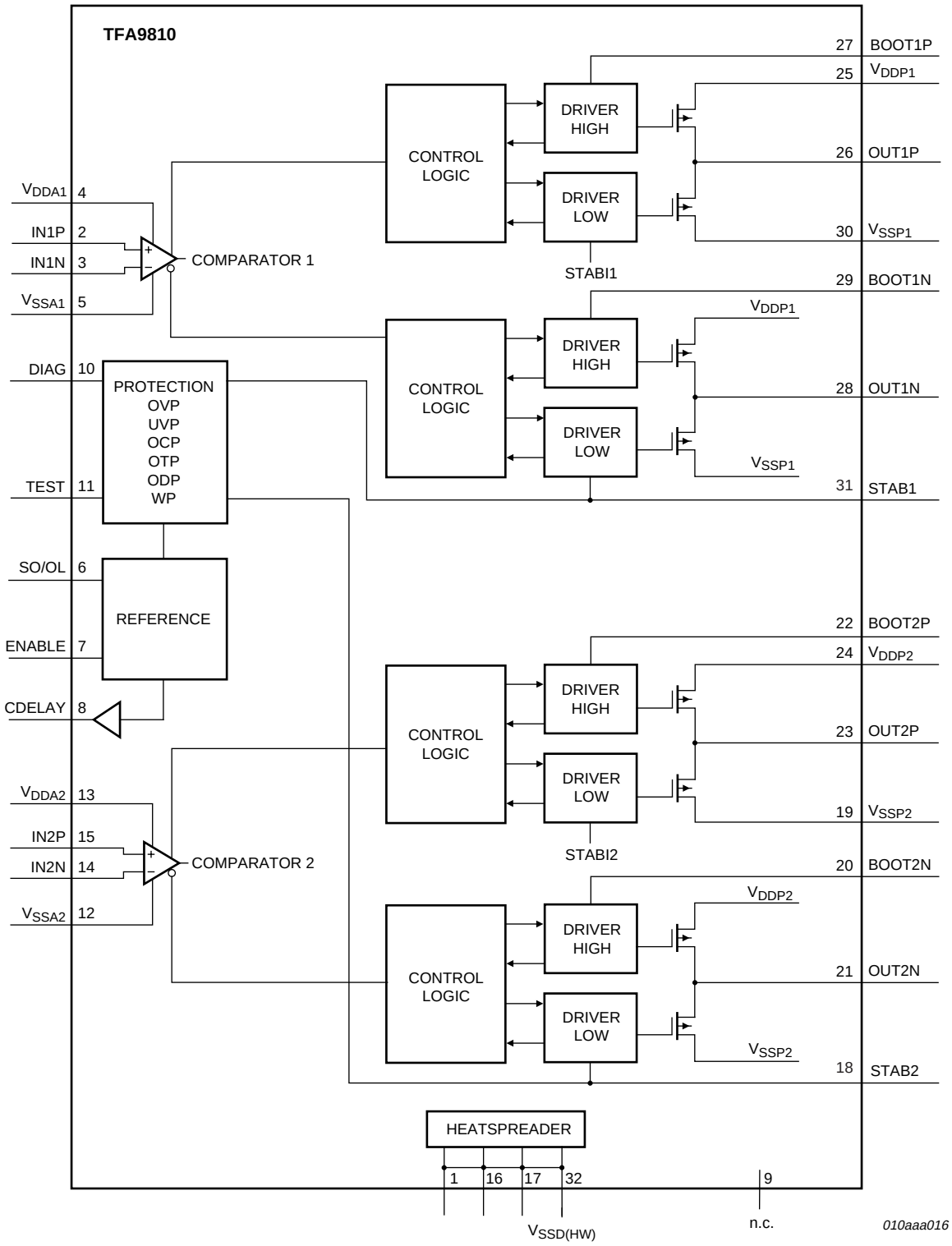


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

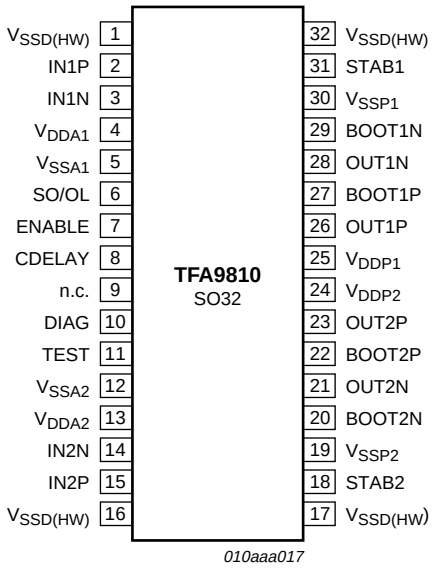


Fig 2. Pin configuration

The SO32 package has four corner leads. These leads (1, 16, 17, and 32) are internally connected to the die pad and must be connected to V_{SSA} in the application. Together with the applied copper area on the Printed Circuit Board (PCB) these leads determine the ambient temperature, which affects the thermal resistance of the junction.

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{SSD(HW)}$	1, 16, 17, 32	Negative digital supply voltage and handle wafer
IN1P	2	Positive input comparator channel 1
IN1N	3	Negative input comparator channel 1
V_{DDA1}	4	Positive analog supply voltage channel 1
V_{SSA1}	5	Negative analog supply voltage channel 1
SO/OL	6	SO/OL input enables self-oscillating / open-loop configuration
ENABLE	7	Enable input to switch between SLEEP and OPERATING
CDELAY	8	CDELAY input determines the switch on/off timing
n.c.	9	Not connected
DIAG	10	Diagnostic output; open drain
TEST	11	Test signal input; for testing purposes only
V_{SSA2}	12	Negative analog supply voltage channel 2
V_{DDA2}	13	Positive analog supply voltage channel 2

Table 3. Pin description *...continued*

Symbol	Pin	Description
IN2N	14	Negative input comparator channel 2
IN2P	15	Positive input comparator channel 2
STAB2	18	Decoupling of internal 11 V regulator for channel 2 drivers
V_{SSP2}	19	Negative power-supply voltage channel 2
BOOT2N	20	Bootstrap high-side driver negative output channel 2
OUT2N	21	Negative output channel 2
BOOT2P	22	Bootstrap high-side driver positive output channel 2
OUT2P	23	Positive output channel 2
V_{DDP2}	24	Positive supply voltage power channel 2
V_{DDP1}	25	Positive power supply voltage channel 1
OUT1P	26	Positive output channel 1
BOOT1P	27	Bootstrap high-side driver positive output channel 1
OUT1N	28	Negative output channel 1
BOOT1N	29	Bootstrap high-side driver negative output channel 1
V_{SSP1}	30	Negative supply voltage power channel 1
STAB1	31	Decoupling of internal 11 V regulator for channel 1 drivers

8. Functional description

8.1 General

The TFA9810 is a dual-switching power comparator. It is the main building block for a stereo high-efficiency Class D audio power amplifier system. It contains two full-bridge BTL power stages, drive logic, protection-control logic and full differential input comparators and references (see Figure 1). By using this power comparator a compact closed-loop self-oscillating digital amplifier system or open-loop system can be built. A second-order low-pass filter converts the Pulse Width Modulation (PWM) output signal into an analog audio signal across the speaker.

8.2 Interfacing

The pins ENABLE and SO/OL control the operating mode of the TFA9810. Both the ENABLE and the SO/OL pins refer to $V_{SSD(HW)}$.

When the SO/OL pin is connected to V_{SSA} the TFA9810 is in self-oscillating mode: when the SO/OL pin is floating the TFA9810 is in open-loop mode.

The TEST pin needs to be connected to ground in both situations.

Table 4. SO/OL connections

Interfacing	
SO/OL connected to	**CONFIGURATION**
$V_{SSD(HW)}$	Self-oscillating
Open	Open-loop

The device has two modes: SLEEP and OPERATING.

In SLEEP mode the TFA9810 is not biased and has a very low supply current.

When the TFA9810 is set into OPERATING mode the device is started via the start-up sequence, which provides a pop-free start-up behavior. After start-up the reference voltages STAB are present and the outputs start switching.

Table 5. Start-up

Interfacing	
ENABLE [V]	**MODE**
ENABLE < 0.8 V	SLEEP
ENABLE > 3 V	OPERATING

8.3 Input comparators

The input stages have a differential input and are optimized for low noise and low offset. This results in maximum flexibility in the application.

8.3.1 Operating in self-oscillating configuration

The inputs (IN1P, IN1N, IN2P, IN2N) of the comparators are internally set to a voltage level of $0.5V_P$, but only during the start-up sequence. In operating mode the inputs are high-ohmic.

8.3.2 Operating in open-loop configuration

No internal voltages are applied to the inputs. The input pins (IN1P, IN1N, IN2P, IN2N) are pulled down to V_{SSA} level by internal resistors.

8.4 Diagnostic

The DIAG output is an open-drain output. The maximum current is 2 mA. Whenever one of the protections is triggered the DIAG output is activated low. The DIAG output refers to V_{SSD}.

8.5 Protections

Overtemperature, overcurrent, overvoltage, undervoltage, over-dissipation sensors, and window protection are included in the TFA9810. When one of these sensors exceeds its threshold level either the output power stage is switched off and the outputs (OUT1N, OUT1P, OUT2N, OUT2P) become floating, or the TFA9810 shuts down and starts up immediately.

- **OverTemperature Protection (OTP)**

  If the junction temperature (T_j) exceeds a threshold level of about 150 °C then the outputs become floating. The device will start switching again after 5 µs and when the temperature is below 150 °C. This is thermal limitation without audible interruptions.

- **OverCurrent Protection (OCP)**

  If the output current exceeds the maximum output current threshold level the output becomes floating. The device will start switching again after 5 µs. This is current limitation without audible interruptions.

- **OverVoltage Protection (OVP)**

  When the supply voltage applied to the TFA9810 exceeds the maximum supply voltage threshold level the device will shut down. The device will restart when the supply voltage is within the operating range.

- **UnderVoltage Protection (UVP)**

  When the supply voltage applied to the TFA9810 falls below the minimum supply voltage threshold level the device will shut down. The device will restart when the supply voltage is within the operating range.

- **Over-Dissipation Protection (ODP)**

  The ODP in the TFA9810 is a combination of two protections. Exceeding a temperature threshold level of 135 °C an internal pre-warning is generated. When an overcurrent is detected during the pre-warning the device will shut down. When the ENABLE pin is high the TFA9810 will restart automatically. The restart sequence (switch-off → switch-on) will take 200 ms to 500 ms.

- **Window Protection (WP)**

  During start-up, if one of the outputs is shorted to V_{SS} or V_{DD} the device will not start. This is an effective measure to protect the device against shorts between the outputs (before the filter) and the ground or supply lines. The supply must be switched off prior to removing any short. The WP protects the device against failure during board assembly.

Table 6. Overview protections

Protections				
Symbol	**Condition**	**DIAG**	**Outputs**	**Recovering**
OTP	T_j > 150 °C	LOW	Floating	Automatic, after 5 µs and T_j < 150 °C
OCP	$I_O > I_{ORM}$	LOW	Floating	Automatic, after 5 µs and $I_O < I_{ORM}$
OVP	V_P > 20 V	LOW	Floating	Restart (switch-off → switch-on when V_P < 20 V)
UVP	V_P < 8 V	LOW	Floating	Restart (switch-off → switch-on when V_P > 8 V)
ODP	T_j > 135 °C and $I_O > I_{ORM}$	LOW	Floating	Restart (switch-off → switch-on when T_j < 135 °C or $I_O < I_{ORM}$)
WP	OUTX > V_{DDA} - 1 V or OUTX < V_{SSA} + 1 V	LOW		

8.6 Start-up sequence

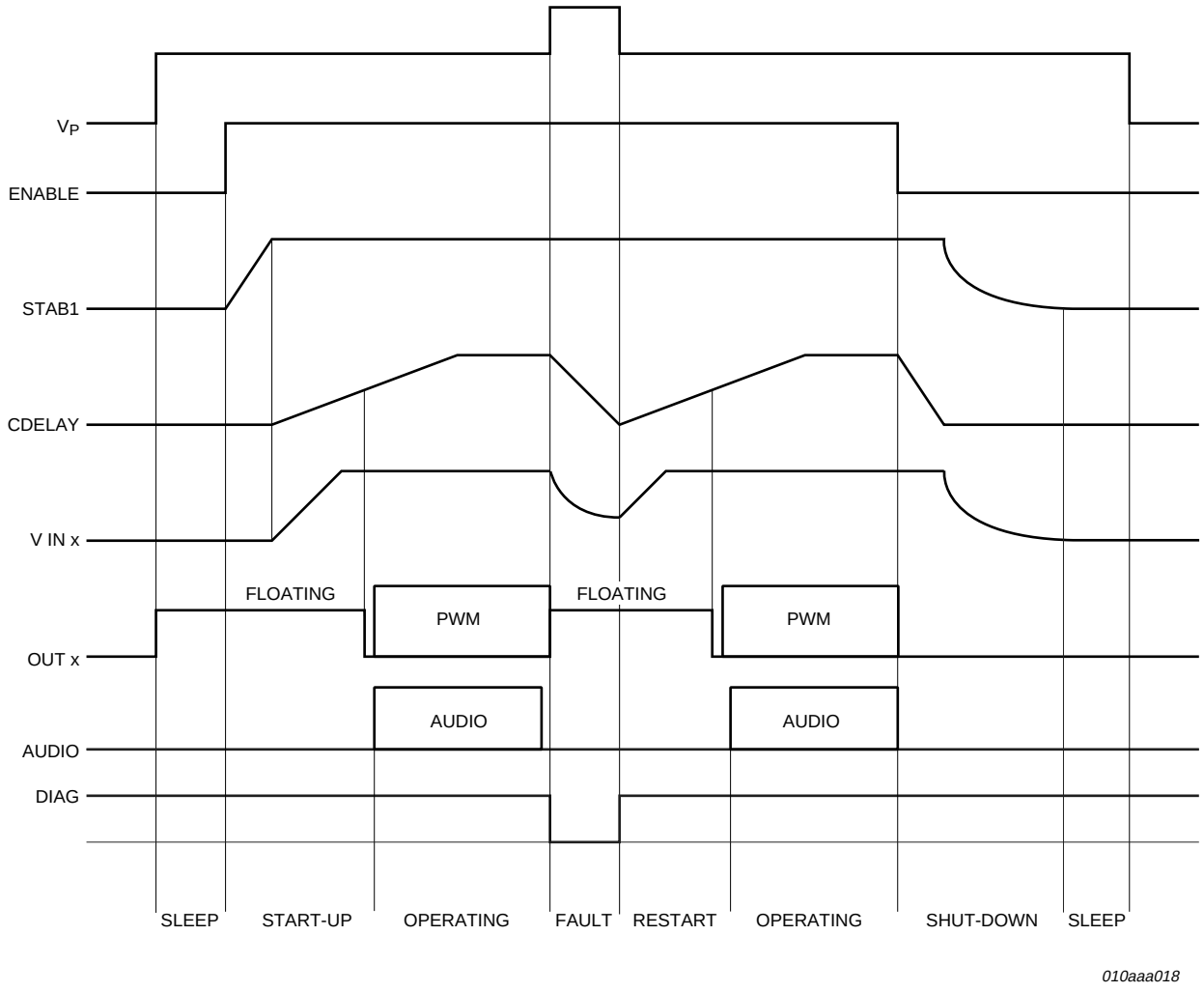


Fig 3. Start-up sequence

9. Internal circuitry

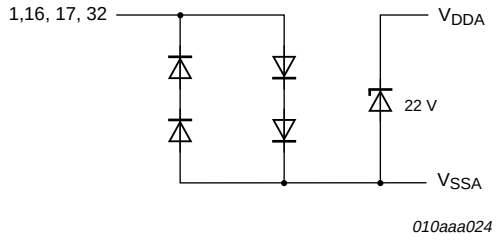


Fig 4. Internal circuitry 0001

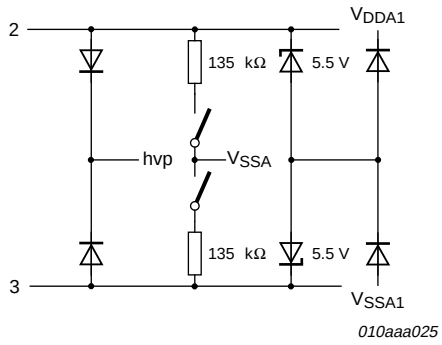


Fig 5. Internal circuitry 0002

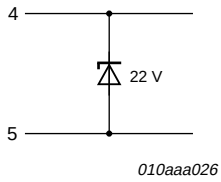


Fig 6. Internal circuitry 0003

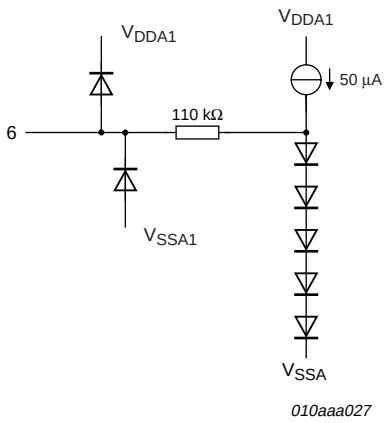


Fig 7. Internal circuitry 0004

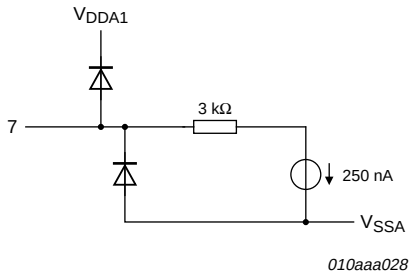


Fig 8. Internal circuitry 0005

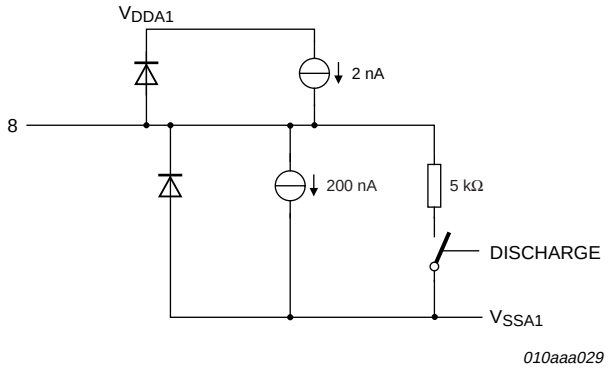


Fig 9. Internal circuitry 0006

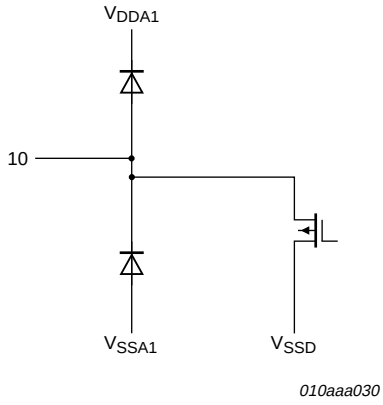


Fig 10. Internal circuitry 0007

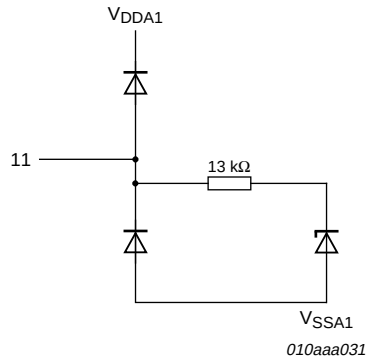


Fig 11. Internal circuitry 0008

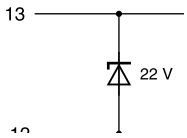


Fig 12. Internal circuitry 0009

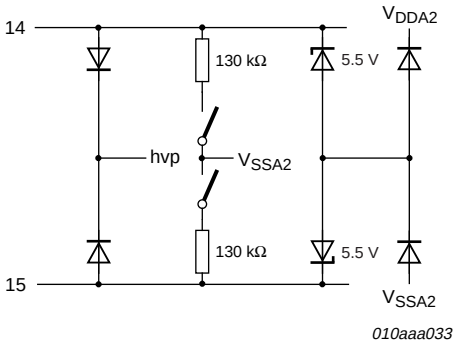


Fig 13. Internal circuitry 0010

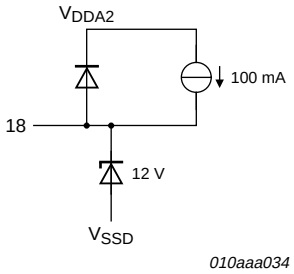


Fig 14. Internal circuitry 0011

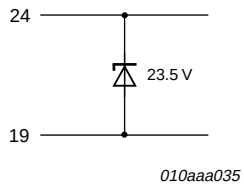


Fig 15. Internal circuitry 0012

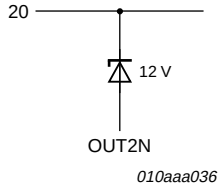


Fig 16. Internal circuitry 0013

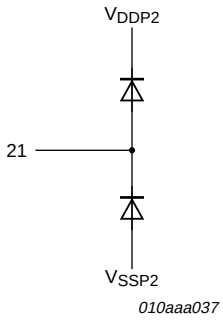


Fig 17. Internal circuitry 0014

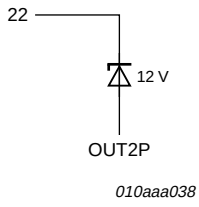


Fig 18. Internal circuitry 0015

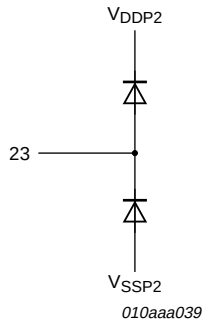


Fig 19. Internal circuitry 0016

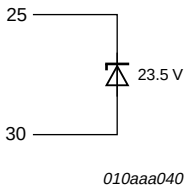


Fig 20. Internal circuitry 0017

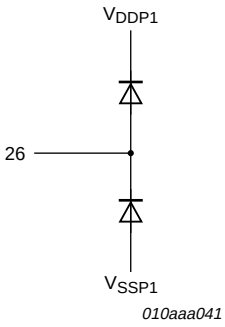


Fig 21. Internal circuitry 0018

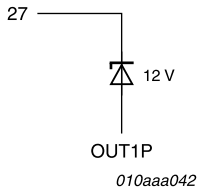


Fig 22. Internal circuitry 0019

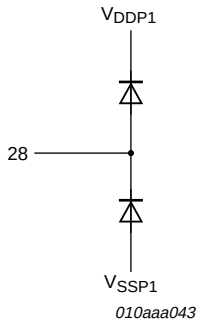


Fig 23. Internal circuitry 0020

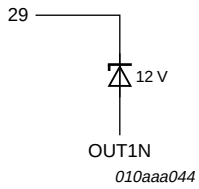


Fig 24. Internal circuitry 0021

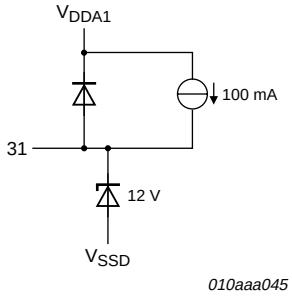


Fig 25. Internal circuitry 0022

10. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_P	supply voltage	asymmetrical	–0.3	+23	V
I_{ORM}	repetitive peak output current		3	-	A
T_j	junction temperature		-	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
P_{max}	maximum power dissipation		-	2.5	W

Table 7. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_x	voltage on pin x	DIAG	V_{SS} – 0.3	+12	V
		IN1P - IN1N	–12	+12	V
		IN2P - IN2N	–12	+12	V
		all other pins	V_{SS} – 0.3	V_{DD} + 0.3	V
V_{esd}	electrostatic discharge voltage	VINX with respect to other pins	–1500	+1500	V
		all other pins	–2000	+2000	V

11. Thermal characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO32. JEDEC test board	[1]	-	41	44	K/W
		SO32. Two-layer application board		-	44	-	K/W
Ψ_{j-lead}	thermal characterization parameter from junction to lead	SO32	[1]			30	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SO32	[1] [2]		4	8	K/W

[1] Measured in a JEDEC high K-factor test board (standard EIA/JESD 51-7) in free air with natural convection.

[2] Strongly depends on where the measurement is taken on the case.

12. Characteristics

12.1 Static characteristics

Table 9. Static characteristics

T_{amb} = 25 °C; V_P = 12 V; f_{osc} = 550 kHz; Figure 33 unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_P	supply voltage	$V_P = V_{DDPx} - V_{SSPx}$	8	12	20	V
I_{off}	off-state current	off mode	-	110	200	µA
I_q	quiescent current	with load, filter, and snubbers connected	-	35	45	mA
ENABLE input						
V_{IL}	LOW-level input voltage	with respect to V_{SSD}	–0.3	-	+0.8	V
V_{IH}	HIGH-level input voltage	with respect to V_{SSD}	3	-	V_P	V

Table 9. Static characteristics *...continued*

T_{amb} = 25 °C; V_P = 12 V; f_{osc} = 550 kHz; Figure 33 unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_I	input current	V_I = 5 V		-	1	20	µA
SO/OL input							
V_{IL}	LOW-level input voltage	with respect to V_{SSD}		-	-	0.4	V
V_{IH}	HIGH-level input voltage	with respect to V_{SSD}		3	4	4.5	V
STABI							
V_{STABI}	voltage on pin STABI	with respect to V_{SS}		10	11	12	V
Comparator full-differential input stage							
$V_{offset(i)(eq)}$	equivalent input offset voltage			-	-	1	mV
		20 Hz < f < 20 kHz		-	-	15	µV
V_{cm}	common mode voltage			V_{SSA} + 3	-	V_{DDA} −1	V
I_{IB}	input bias current			-	-	1	µA
OverTemperature Protection (OTP)							
T_{prot}	protection temperature			150	-	-	°C
OverVoltage Protection (OVP)							
$V_{th(ovp)}$	overvoltage protection threshold voltage	level internal fixed		20	21.5	23	V
UnderVoltage Protection (UVP)							
$V_{P(uvp)}$	undervoltage protection supply voltage	level internal fixed		7	7.5	8	V
OverCurrent Protection (OCP)							
$I_{O(ocp)}$	overcurrent protection output current		[1]	3	3.5	-	A
Window Protection (WP)							
V_O	output voltage	high level		-	V_{DDA} − 1	-	V
		low level		-	V_{SSA} + 1	-	V

[1] Current limiting concept: in overcurrent condition no interruption of the audio signal in case of impedance drop.

12.2 Dynamic characteristics

Table 10. Dynamic characteristics

T_{amb} = 25 °C; V_P = 12 V; R_L = 8 Ω; Figure 33 unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PWM Output							
t_r	rise time			-	10	-	ns
t_f	fall time			-	10	-	ns
t_{resp}	response time	transition PWM output from LOW to HIGH		-	60	-	ns
		V_I = 70 mV		-	50	-	ns
		V_I = 3.3 V					
		transition PWM output from HIGH to LOW		-	60	-	ns
		V_I = 70 mV		-	50	-	ns
		V_I = 3.3 V					
$t_{w(min)}$	minimum pulse width	PWM output		-	60	-	ns
R_{DSon}	drain-source on-state resistance		[1]	-	0.28	0.35	Ω
η_{po}	output power efficiency	output power 2 x 9 W into 8 Ω. $P_o = P_{o(nom)}$	[2]	87	89	-	%

[1] High-side and low-side power switch have the same series resistance.

[2] Output power measured across the loudspeaker load. Output power is measured indirectly via R_{DSon}.

12.3 AC characteristics measured in a typical application

Table 11. AC characteristics measured in typical application

T_{amb} = 25 °C; V_P = 12 V; R_L = 8 Ω; f_{osc} = 550 kHz; Figure 33 unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_P	operating supply voltage	$V_P = V_{DDPx} - V_{SSPx}$	8	12	20	V
$P_{o(RMS)}$	continuous RMS output power per channel.	R_L = 8 Ω; V_P = 12 V THD = 10 %; Two channel driven; no heat sink required.	-	9.5	-	W
P_o	output power	V_P =12 V; R_L= 8 Ω	-	-	-	W
		THD = 10 %	8.5	9.5	-	W
		THD = 1 %	6.5	7.5	-	W
		V_P = 14 V; R_L = 8 Ω; THD = 10 %; thermally limited	-	12	-	W
		V_P = 16 V; R_L = 8 Ω; THD = 10 %; thermally limited	-	15	-	W
		V_P = 12 V; R_L = 6 Ω; THD = 10 %; thermally limited	-	12	-	W
		R_L = 4 Ω; V_P = 12 V; THD = 10 %; thermally limited	-	15	-	W

Table 11. AC characteristics measured in typical application *...continued*

T_{amb} = 25 °C; V_P = 12 V; R_L = 8 Ω; f_{osc} = 550 kHz; Figure 33 unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD+N	total harmonic distortion-plus-noise	P_o is 1 W; f = 1 kHz; AES17 brick-wall filter		-	0.04	0.1	%
η_{po}	output power efficiency	P_o = 9 W		87	89	-	%
$G_{v(cl)}$	closed-loop voltage gain	V_I = 100 mV (RMS); f_i = 1 kHz		19	19.7	21	dB
$V_{n(o)}$	noise output voltage	Inputs shorted; AES17 brick-wall filter		-	150	-	μV
S/N	signal-to-noise ratio	V_o = 10 V(RMS); gain 20 dB		-	96	-	dB
SVRR	supply voltage ripple rejection	V_{ripple} = 2 Vpp; f_I= 1kHz	[1]	34	45	-	dB
α_{cs}	channel separation	P_o = 1 W; f_i = 1 kHz		55	70	-	dB

[1] Minimum value determined by R5, R10, R17, R22 equalling +1 % and R7, R14, R18, R20 equalling –1 %.

13. Quality specification

In accordance with SNW-FQ-611-E, 'if this type is used as an audio amplifier'. The number of the quality specification can be found in the Quality Reference Handbook. The handbook can be ordered using the code 9398 510 63011.

14. Application information

14.1 Output power estimation

For BTL configuration the output power just before clipping can be estimated using Equation 1:

$$BTL: P_{o0.5\,\%} = \frac{\left[\left[\frac{R_L}{R_L + 2 \times (R_{DSon} + R_s)}\right] \times V_P\right]^2}{2 \times R_L} \quad (1)$$

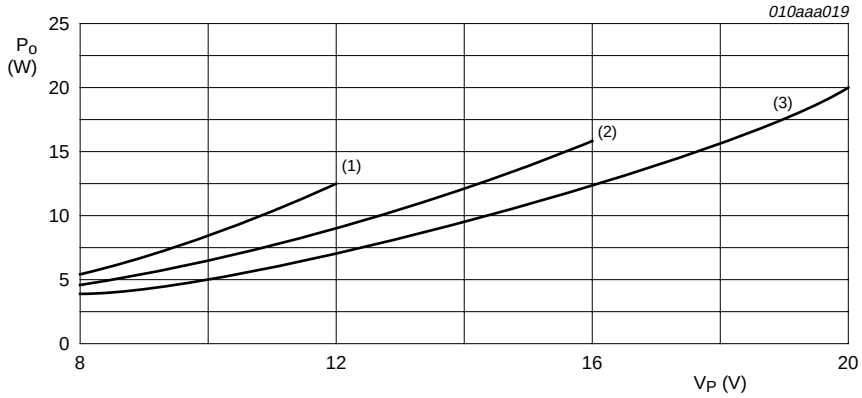
Where,

- V_P = supply voltage ($V_{DDPx} - V_{SSPx}$) [V]
- R_L = load resistance [Ω]
- R_{DSon} = drain-source on-state resistance [Ω]
- R_s = series resistance [Ω]
- $P_{o0.5\,\%}$ = output power at the THD level of 0.5 % [W]

The output power at 10 % THD can be estimated by using Equation 2:

$$P_{o10\,\%} = 1.25 \times P_{o0.5\,\%} \quad (2)$$

Figure 26 and Figure 27 below show the estimated output power at THD = 0.5 % and THD = 10 % as a function of the BLT supply voltage for different load impedances.

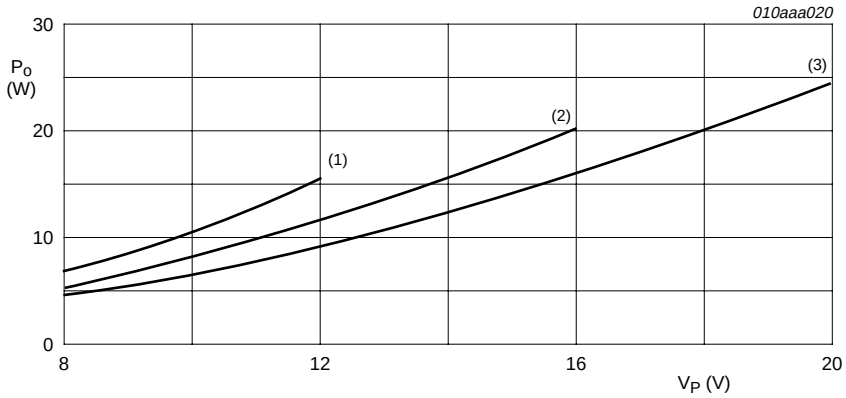


(1) R_L = 4 Ω

(2) R_L = 6 Ω

(3) R_L = 8 Ω

Fig 26. BTL output power as function of supply voltage: THD = 0.5 %. 3 A



(1) R_L = 4 Ω

(2) R_L = 6 Ω

(3) R_L = 8 Ω

Fig 27. BTL output power as function of supply voltage: THD = 10 %. 3 A

14.2 Output current limiting

The peak output current is internally limited above a level of 3 A minimum. During normal operation the output current should not exceed this threshold level of 3 A, otherwise the output signal will be distorted. The peak output current in BTL can be estimated using Equation 3:

$$I_O max \leq \frac{V_P}{R_L + 2 \times (R_{DSon} + R_s)} \leq 3\ A \quad (3)$$

Where:

- V_P = supply voltage ($V_{DDPx} - V_{SSPx}$) [V].
- R_L = load resistance [Ω].
- R_{DSon} = drain-source on-state resistance [Ω].
- R_s = series resistance [Ω].

Example:

A 4 Ω speaker in BTL configuration can be used up to a supply voltage of 12 V without running into current limiting. Current limiting (clipping) will avoid audio holes, but it causes a sound distortion similar to voltage clipping.

14.3 Speaker configuration and impedance

For a flat-frequency response (second-order Butterworth filter) it is necessary to change the low-pass filter components L_{LC} and C_{LC} according to the speaker configuration and impedance. Table 12 shows the practical required values:

Table 12. Filter component values

Configuration	Impedance [Ω]	L_{LC} [μF]	C_{LC} [nF]
BTL	4	10	1500
	6	16	1000
	8	22	680

14.4 Differential input

For a high common-mode rejection ratio and a maximum of flexibility in the application, the audio inputs of the application are fully differential.

The input configuration for a differential-input application is illustrated in Figure 28.

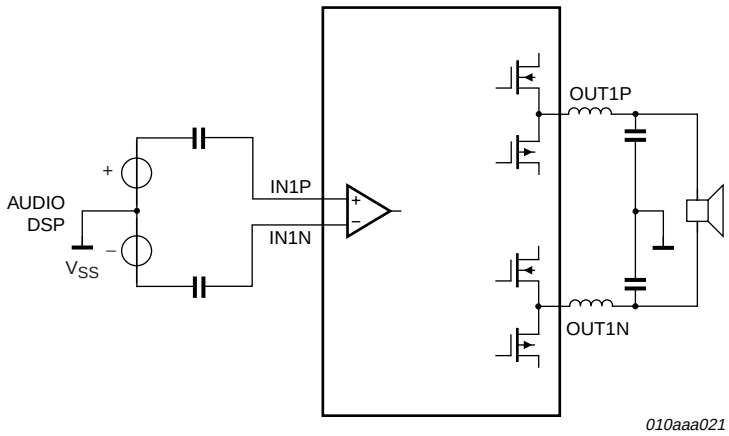


Fig 28. Input configuration for differential input

14.5 Single-ended input

When using an audio source with a single-ended ‘out’, it is important to connect the IN1N from the application board to the VSS/GND of the audio source (e.g. Audio DSP).

The input configuration for single-ended ‘in’ application is illustrated in Figure 29.

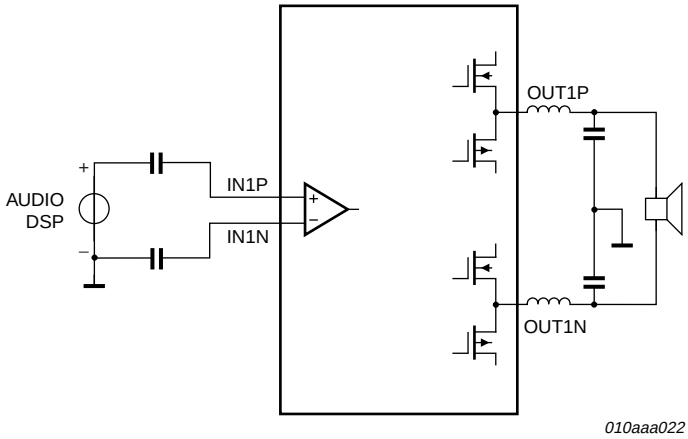
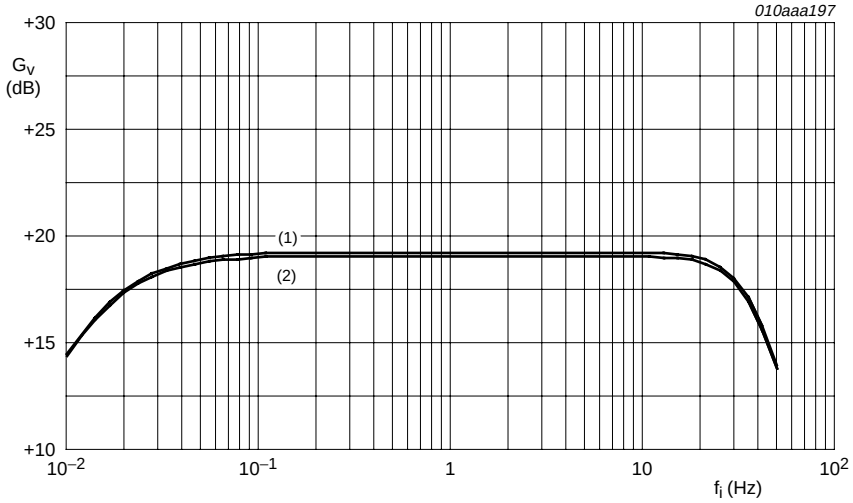


Fig 29. Input configuration for single-ended input

14.6 Curves measured in a typical application

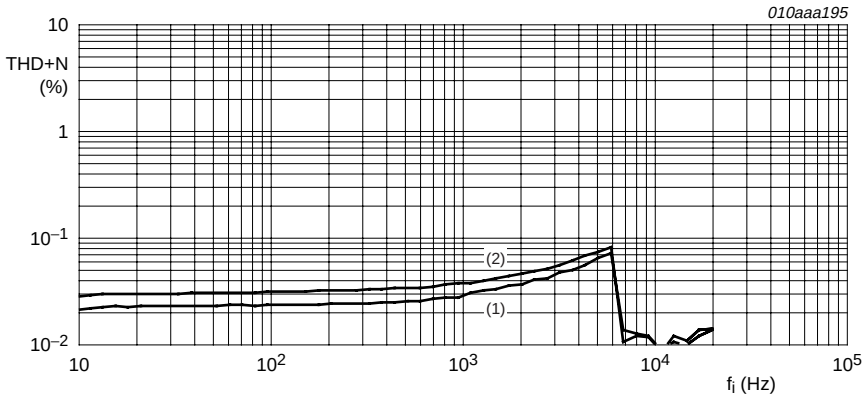


V_P = 12 V, V_i = 100 mV

(1) OUT1

(2) OUT2

Fig 30. Gain as a function of frequency

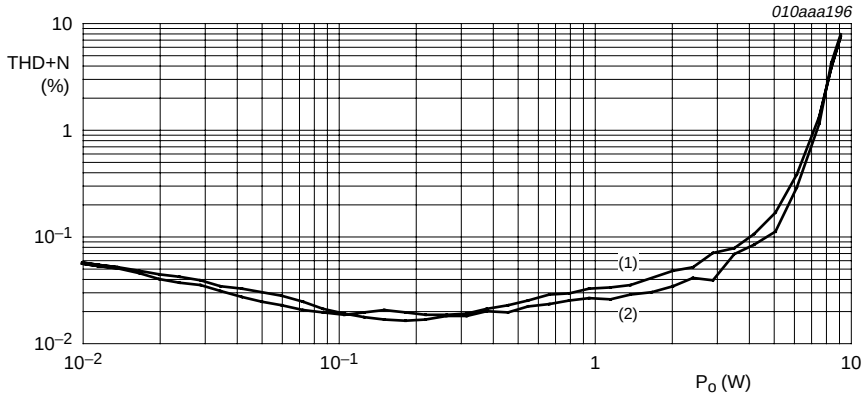


V_P = 12 V, R_L = 8 Ω, P_o = 1 W

(1) OUT1

(2) OUT2

Fig 31. Total harmonic distortion + noise as a function of frequency



V_P = 12 V, R_L = 8 Ω, f_i = 1 kHz

(1) OUT1

(2) OUT2

Fig 32. Total harmonic distortion as a function of output power

14.7 Typical application diagram TFA9810

The typical application diagram with the TFA9810 supplied from an asymmetrical supply is shown in Figure 33.

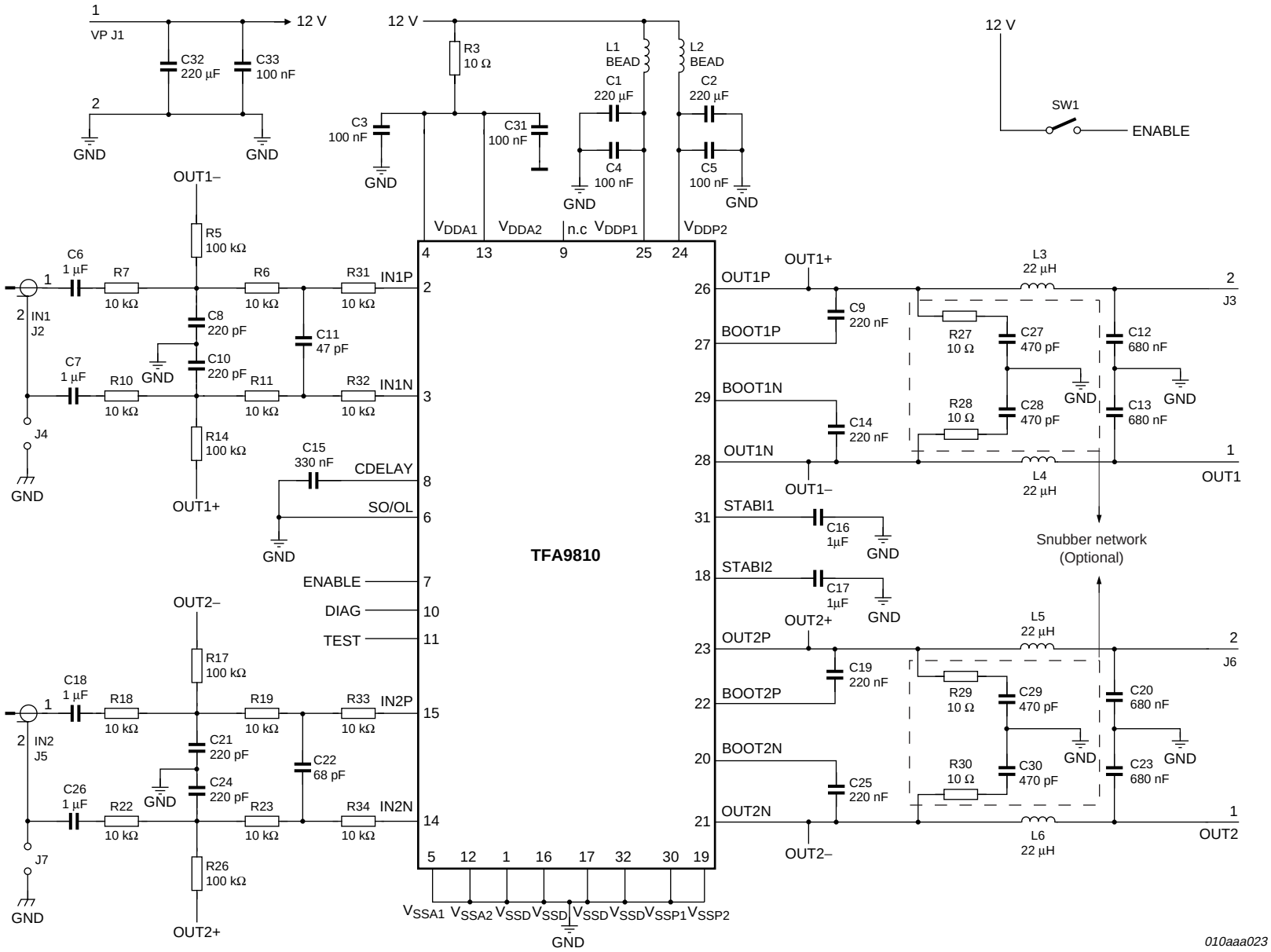


Fig 33. Typical application diagram TFA9810

14.8 Typical application: bill of materials

Table 13. Typical application: bill of materials

Item	Quantity	Reference	Part	Description
1	2	C1, C2.	220 µF/35 V	General purpose 85 °C, diameter 8 mm
2	5	C3, C4, C5, C31, C33.	100 nF/50 V	SMD 0805 X7R
3	2	C16, C17.	1 µF/50 V	SMD 1206 X7R
4	4	C6, C7, C18, C26	1 µF/25 V	MKT
5	4	C8, C10, C21, C24.	220 pF/25 V	SMD 0402 NP0
6	4	C9, C14, C19, C25.	220 nF/25 V	SMD 0805 X7R
7	1	C11	47 pF/25 V	SMD 0402 NP0
8	4	C12, C13, C20, C23.	680 nF/25 V	MKT
9	1	C15	330 nF/25 V	SMD 0805 X7R
10	1	C22.	68 pF/25 V	SMD 0402 NP0
11	1	C32	1000 µF/25 V	CE12-02R
12	3	J1, J3, J6.	Screw terminal	Two pins
13	2	J2, J5.	CINCH	CINCH
14	2	J4, J7	Jumper	Closed on demo board only
15	2	L1, L2.	BEAD	SMD 1206 Würth Elektronik DC < 0.5 Ω 10 MHz > 80 Ω
16	4	L3, L4, L5, L6.	22 µH	8RDY TOKO A7040HN-220M, 11RHBP TOKO A7503CY-220M or Sagami 7311NA-220M
17	5	R3	10 / 0.25 W / 5 %	SMD 1206
18	4	R5, R14, R17, R26.	100 k / 0.1 W / 1 % for 20 dB 200 k / 0.1 W / 1 % for 26 dB	SMD 0603
19	12	R6, R7, R10, R11, R18, R19, R22, R23, R31, R32, R33, R34.	10 k / 0.1 W / 1 %	SMD 0603
20	1	SW1	PCB switch	Secme 090320901
21	1	U1	TFA9810T	SOT287-1 (SO32) NXP Semiconductors

14.9 Snubber network

Table 14. Snubber network: bill of materials

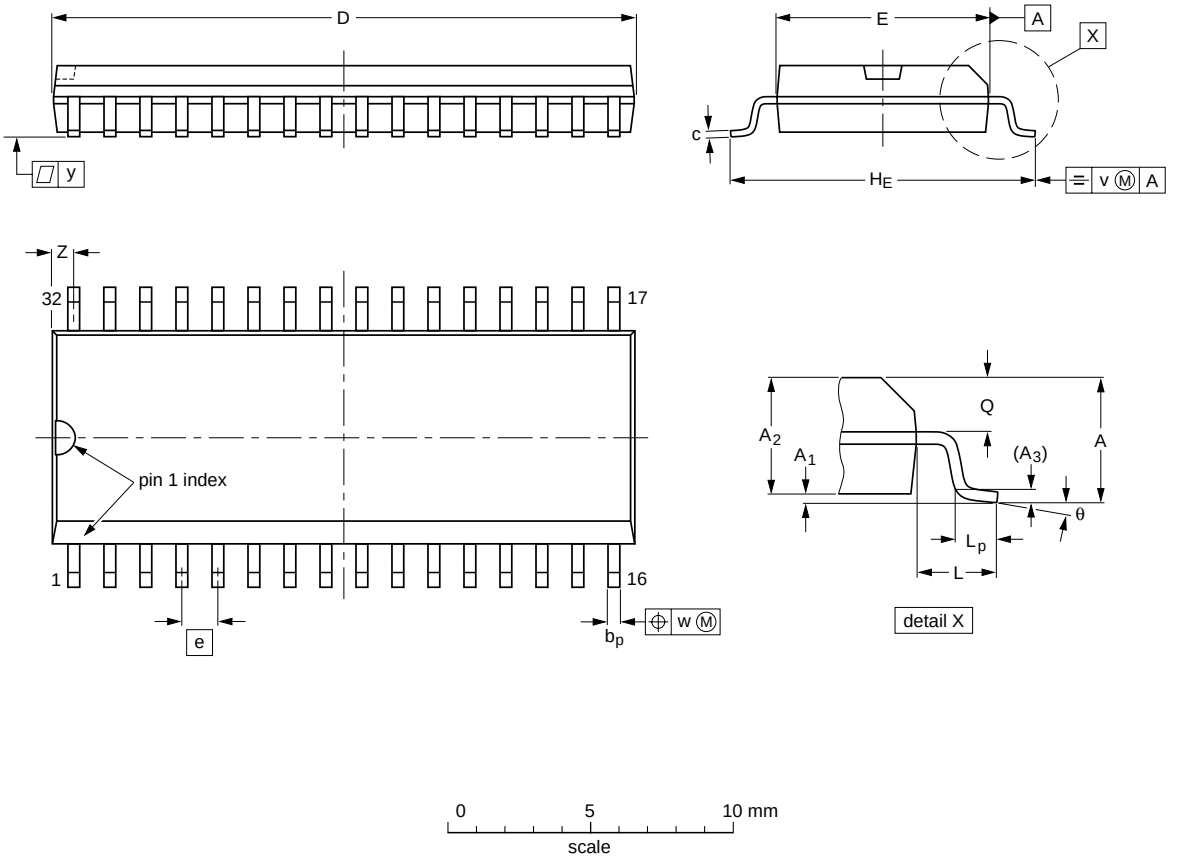
Item	Quantity	Reference	Part	Footprint
1	4	C27, C28, C29, C30	470 pF, 25 V	SMD 0805 X7R
2	4	R27, R28, R29, R30	10 / 0.25 W / 5 %	SMD 1206

15. Test information

General Quality Specification for General Applications, Power management and RF Power. Document SNW-FQ-611 refers.

16. Package outline

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT287-1		MO-119				~~00-08-17~~ 03-02-19

Fig 34. Package outline

17. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9810_2	20070830	Preliminary data sheet	-	TFA9810_1
Modifications:	• Added legal statement on “Right to make changes” in Section 18.3.			
TFA9810_1	20070815	Preliminary data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

18.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

20. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 30 August 2007
Document identifier: TFA9810_2